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58. (New) The integrated circuit of claim 55, wherein the first layer of material includes germanium.

59. (New) The integrated circuit of claim 55, wherein the second layer includes titanium nitride.

60. (New) The integrated circuit of claim 55, wherein the second layer includes a barrier layer material.

61. (New) The integrated circuit of claim 55, wherein the first layer and the second layer have a thickness on the order of 100 to 500 Å.

62. (New) The integrated circuit of claim 55, wherein the copper metallization layer fills the contact vias.

63. (New) The integrated circuit of claim 55, wherein the first layer has a first surface voltage, the second layer has a second surface voltage, and the first surface voltage is lower than the second surface voltage.

64. (New) An integrated circuit, comprising:

a substrate;

a first layer of material formed on the substrate, the first layer having contact vias extending through to the substrate, the first layer having a first surface voltage;

a second layer formed on the first layer, the second layer lining the contact vias, the second layer having a second surface voltage; and

a copper metallization layer formed on the second layer.

65. (New) The integrated circuit of claim 64, wherein the first layer of material includes doped polysilicon.

66. (New) The integrated circuit of claim 64, wherein the first layer of material includes undoped polysilicon.

67. (New) The integrated circuit of claim 64, wherein the first layer of material includes germanium.

68. (New) The integrated circuit of claim 64, wherein the second layer includes titanium nitride.

69. (New) The integrated circuit of claim 64, wherein the second layer includes a barrier layer material.

70. (New) The integrated circuit of claim 64, wherein the first layer and the second layer have a thickness on the order of 100 to 500 Å.

71. (New) The integrated circuit of claim 64, wherein the copper metallization layer fills the contact vias.

72. (New) The integrated circuit of claim 64, wherein the first surface voltage is lower than the second surface voltage.

73. (New) An integrated circuit, comprising:

a substrate;

a first layer of material formed on the substrate, the first layer having contact vias extending through to the substrate;

a second layer formed on the first layer, the second layer lining the contact vias; and

a nickel metallization layer formed on the second layer.

74. (New) The integrated circuit of claim 73, wherein the first layer of material includes doped polysilicon.

75. (New) The integrated circuit of claim 73, wherein the first layer of material includes undoped polysilicon.

76. (New) The integrated circuit of claim 73, wherein the first layer of material includes germanium.

77. (New) The integrated circuit of claim 73, wherein the second layer includes titanium nitride.

78. (New) The integrated circuit of claim 73, wherein the second layer includes a barrier layer material.

79. (New) The integrated circuit of claim 73, wherein the first layer and the second layer have a thickness on the order of 100 to 500 Å.

80. (New) The integrated circuit of claim 73, wherein the nickel metallization layer fills the contact vias.

81. (New) The integrated circuit of claim 73, wherein the first layer has a first surface voltage, the second layer has a second surface voltage, and the first surface voltage is lower than the second surface voltage.

82. (New) An integrated circuit, comprising:

a substrate;

a first layer of material formed on the substrate, the first layer having contact vias extending through to the substrate;

a second layer formed on the first layer, the second layer lining the contact vias; and

a palladium metallization layer formed on the second layer.

83. (New) The integrated circuit of claim 82, wherein the first layer of material includes doped polysilicon.

84. (New) The integrated circuit of claim 82, wherein the first layer of material includes undoped polysilicon.

85. (New) The integrated circuit of claim 82, wherein the first layer of material includes germanium.

86. (New) The integrated circuit of claim 82, wherein the second layer includes titanium nitride.

87. (New) The integrated circuit of claim 82, wherein the second layer includes a barrier layer material.

88. (New) The integrated circuit of claim 82, wherein the first layer and the second layer have a thickness on the order of 100 to 500 Å.

89. (New) The integrated circuit of claim 82, wherein the palladium metallization layer fills the contact vias.

90. (New) The integrated circuit of claim 82, wherein the first layer has a first surface voltage, the second layer has a second surface voltage, and the first surface voltage is lower than the second surface voltage.

91. (New) An integrated circuit, comprising:

a substrate;

a borophosphosilicate glass (BPSG) layer formed on the substrate;

a first layer of material formed on the BPSG layer, the first layer having contact vias extending through the BPSG layer to the substrate;

a second layer formed on the first layer, the second layer lining the contact vias; and

a metallization layer formed on the second layer.

13 ~~92.~~ 12 (New) The integrated circuit of claim ~~91~~, wherein the first layer of material includes doped polysilicon.

14 ~~93.~~ 12 (New) The integrated circuit of claim ~~91~~, wherein the first layer of material includes undoped polysilicon.

15 ~~94.~~ 12 (New) The integrated circuit of claim ~~91~~, wherein the first layer of material includes germanium.

16 ~~95.~~ 12 (New) The integrated circuit of claim ~~91~~, wherein the second layer includes titanium nitride.

17 ~~96.~~ 12 (New) The integrated circuit of claim ~~91~~, wherein the second layer includes a barrier layer material.

18 ~~97.~~ 12 (New) The integrated circuit of claim ~~91~~, wherein the first layer and the second layer have a thickness on the order of 100 to 500 Å.

19 ~~98.~~ 12 (New) The integrated circuit of claim ~~91~~, wherein the metallization layer fills the contact vias.

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99. (New) The integrated circuit of claim 91, wherein the first layer has a first surface voltage, the second layer has a second surface voltage, and the first surface voltage is lower than the second surface voltage.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612-373-6960) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

GURTEJ SINGH SANDHU ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6960

Date 6-22-01 By Marvin L Beek

Marvin L. Beekman
Reg. No. 38,377

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 22nd day of June, 2001.

Name Amy Moriarty

Signature Amy Moriarty

Clean Version of Pending Claims

METHOD FOR FORMING A METALLIZATION LAYER
Applicant: Gurtej Singh Sandhu et al.
Serial No.: 09/652,619

Claims 21-31 and 55-99, as of June 22, 2001 (response to restriction requirement).

21. An integrated circuit, comprising:

a substrate;

a first layer of material formed on the substrate, the first layer having contact vias extending through to the substrate;

a second layer formed on the first layer, the second layer lining the contact vias; and

a metallization layer on the second layer.

22. The integrated circuity of claim 21, wherein the metallization layer comprises non-alloy copper.

23. The integrated circuitry of claim 21, wherein the metallization layer fills the contact vias.

24. The integrated circuitry of claim 21, wherein the first layer has a first surface potential and the second layer has a second surface potential, and wherein the first surface potential is lower than the second surface potential.

25. An integrated circuit, comprising:

a substrate;

a first layer of material formed on the substrate, the first layer having a first surface voltage;

a second layer of material formed on the first layer, the second layer having a second surface voltage, the second surface voltage being different than the first surface voltage; and

a metallization layer formed on the second layer.

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26. The integrated circuit of claim 25, wherein the metallization layer comprises non-alloy copper.

27. The integrated circuit of claim 25, wherein the first layer comprises poly-silicon and the second layer comprises titanium nitride.

28. The integrated circuit of claim 25, wherein the first surface voltage is lower than the second surface voltage.

29. An integrated circuit, comprising:

a substrate;

a first layer of material formed on the substrate;

an insulator layer formed on the first layer, the insulator layer and the first layer having contact vias;

a second layer formed on the first layer, the second layer lining the contact vias; and

a metallization layer on the second layer.

30. The integrated circuit of claim 29, wherein the metallization layer on the second layer fills the contact vias.

31. The integrated circuit of claim 29, wherein the first layer and the second layer have exposed surfaces upon which voltage may be applied.

55. (New) An integrated circuit, comprising:

a substrate;

a first layer of material formed on the substrate, the first layer having contact vias extending through to the substrate;

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a second layer formed on the first layer, the second layer lining the contact vias; and

a copper metallization layer formed on the second layer.

56. (New) The integrated circuit of claim 55, wherein the first layer of material includes doped polysilicon.

57. (New) The integrated circuit of claim 55, wherein the first layer of material includes undoped polysilicon.

58. (New) The integrated circuit of claim 55, wherein the first layer of material includes germanium.

59. (New) The integrated circuit of claim 55, wherein the second layer includes titanium nitride.

60. (New) The integrated circuit of claim 55, wherein the second layer includes a barrier layer material.

61. (New) The integrated circuit of claim 55, wherein the first layer and the second layer have a thickness on the order of 100 to 500 Å.

62. (New) The integrated circuit of claim 55, wherein the copper metallization layer fills the contact vias.

63. (New) The integrated circuit of claim 55, wherein the first layer has a first surface voltage, the second layer has a second surface voltage, and the first surface voltage is lower than the second surface voltage.

64. (New) An integrated circuit, comprising:

a substrate;

a first layer of material formed on the substrate, the first layer having contact vias extending through to the substrate, the first layer having a first surface voltage;

a second layer formed on the first layer, the second layer lining the contact vias, the second layer having a second surface voltage; and

a copper metallization layer formed on the second layer.

65. (New) The integrated circuit of claim 64, wherein the first layer of material includes doped polysilicon.

66. (New) The integrated circuit of claim 64, wherein the first layer of material includes undoped polysilicon.

67. (New) The integrated circuit of claim 64, wherein the first layer of material includes germanium.

68. (New) The integrated circuit of claim 64, wherein the second layer includes titanium nitride.

69. (New) The integrated circuit of claim 64, wherein the second layer includes a barrier layer material.

70. (New) The integrated circuit of claim 64, wherein the first layer and the second layer have a thickness on the order of 100 to 500 Å.

71. (New) The integrated circuit of claim 64, wherein the copper metallization layer fills the

contact vias.

72. (New) The integrated circuit of claim 64, wherein the first surface voltage is lower than the second surface voltage.

73. (New) An integrated circuit, comprising:

a substrate;

a first layer of material formed on the substrate, the first layer having contact vias extending through to the substrate;

a second layer formed on the first layer, the second layer lining the contact vias; and

a nickel metallization layer formed on the second layer.

74. (New) The integrated circuit of claim 73, wherein the first layer of material includes doped polysilicon.

75. (New) The integrated circuit of claim 73, wherein the first layer of material includes undoped polysilicon.

76. (New) The integrated circuit of claim 73, wherein the first layer of material includes germanium.

77. (New) The integrated circuit of claim 73, wherein the second layer includes titanium nitride.

78. (New) The integrated circuit of claim 73, wherein the second layer includes a barrier layer material.

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79. (New) The integrated circuit of claim 73, wherein the first layer and the second layer have a thickness on the order of 100 to 500 Å.

80. (New) The integrated circuit of claim 73, wherein the nickel metallization layer fills the contact vias.

81. (New) The integrated circuit of claim 73, wherein the first layer has a first surface voltage, the second layer has a second surface voltage, and the first surface voltage is lower than the second surface voltage.

82. (New) An integrated circuit, comprising:

a substrate;

a first layer of material formed on the substrate, the first layer having contact vias extending through to the substrate;

a second layer formed on the first layer, the second layer lining the contact vias; and

a palladium metallization layer formed on the second layer.

83. (New) The integrated circuit of claim 82, wherein the first layer of material includes doped polysilicon.

84. (New) The integrated circuit of claim 82, wherein the first layer of material includes undoped polysilicon.

85. (New) The integrated circuit of claim 82, wherein the first layer of material includes germanium.

86. (New) The integrated circuit of claim 82, wherein the second layer includes titanium

nitride.

87. (New) The integrated circuit of claim 82, wherein the second layer includes a barrier layer material.

88. (New) The integrated circuit of claim 82, wherein the first layer and the second layer have a thickness on the order of 100 to 500 Å.

89. (New) The integrated circuit of claim 82, wherein the palladium metallization layer fills the contact vias.

90. (New) The integrated circuit of claim 82, wherein the first layer has a first surface voltage, the second layer has a second surface voltage, and the first surface voltage is lower than the second surface voltage.

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91. (New) An integrated circuit, comprising:

a substrate;

a borophosphosilicate glass (BPSG) layer formed on the substrate;

a first layer of material formed on the BPSG layer, the first layer having contact vias extending through the BPSG layer to the substrate;

a second layer formed on the first layer, the second layer lining the contact vias; and

a metallization layer formed on the second layer.

92. (New) The integrated circuit of claim 91, wherein the first layer of material includes doped polysilicon.

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93. (New) The integrated circuit of claim 91, wherein the first layer of material includes undoped polysilicon.

94. (New) The integrated circuit of claim 91, wherein the first layer of material includes germanium.

95. (New) The integrated circuit of claim 91, wherein the second layer includes titanium nitride.

96. (New) The integrated circuit of claim 91, wherein the second layer includes a barrier layer material.

97. (New) The integrated circuit of claim 91, wherein the first layer and the second layer have a thickness on the order of 100 to 500 Å.

98. (New) The integrated circuit of claim 91, wherein the metallization layer fills the contact vias.

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~~99.~~ 13 (New) The integrated circuit of claim ~~91~~, wherein the first layer has a first surface voltage, the second layer has a second surface voltage, and the first surface voltage is lower than the second surface voltage.

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